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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,966	06/08/2000	Michael J. Demler	ANTR-01016US1	1467

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FLIESLER DUBB MEYER & LOVEJOY, LLP
FOUR EMBARCADERO CENTER
SUITE 400
SAN FRANCISCO, CA 94111

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2123	11

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/589,966	Michael J. Demler
Examiner	**Art Unit**
Thai Phan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 15, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-10 and 12-24* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-10 and 12-24* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on July 15, 2003. Claim 11 is canceled. Claims 15-24 are newly added. Claims 1-10 and 12-24 are pending in this Office Action.

Drawings

1. The drawings filed on July 15, 2003 have been received and considered.

Information Disclosure Statement

2. The information disclosure statements filed on Dec. 27, 2000 and Apr. 09, 2001 have been considered and placed in the record.

Claim Rejections - 35 USC § 112

3. Due to amendment to claim 12, claim 12 rejection has been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-10 and 12-24 are rejected under 35 U.S.C. 103(a) as being obvious over Hamid, Adnan, US patent no. 5,655,109 in view of Barford et al., US patent no. 5,946,482.

As per claim 1, Hamid discloses a method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the method of planning a circuit synthesis includes steps and means:

determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior by polynomial curve fitting function (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, col. 10, lines 18-25, for example). Such circuit simulation could provide an effective way to simulate

and characterize the design behaviors in the circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 2, Hamid discloses means and step of storing simulation results in storage means. The store formats include tabular form corresponding to each simulation process on a set of points as claimed (Fig. 2).

As per claim 3, Barford teaches polynomial fitted transfer equation over a design parameter values (col. 3, line 46 to col. 4, line 18, col. 10, lines 18-25).

As per claim 4, Hamid disclose analog design as claimed.

As per claim 5, Hamid discloses a method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the method of planning a circuit synthesis includes steps and means:

determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

means for consolidating the simulation results for the design, storing means for storing the consolidated results of the simulation in a behavioral model of the plan, means for selecting plan and a set of performance requirement to the simulation engine, means for executing or simulating the cell characterization plan (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, col. 10, lines 18-25, for example). Such circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 6, Hamid discloses layout patten files which would include netlist files for cells layout.

As per claim 7, Hamid discloses a method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the method of planning a circuit synthesis includes steps and means for:

determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior using polynomial curve fitting techniques (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, col. 10, for example). Such circuit simulation could provide an effective way to simulate and

characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 8, Hamid discloses setting parameters to a fixed value (cols. 5 and 6) for cells characterization, setting values for other parameters for the complete design (cols. 5-6), simulating the circuit design to produce a result (col. 5), varying the parameter information in parameter design space to optimize the design (cols. 4-5), and repeating the steps of varying and simulating for a predetermined number of iteration to optimize the design.

As per claim 9, Barford discloses repeating step of simulating and fitting to produce simulation result, and selecting an optimized circuit solution from the set of simulation data points (cols. 3, 6).

As per claim 10, Hamid discloses a synthesis method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the synthesizer for planning a circuit synthesis includes steps and means:

means configured to determine an optimized circuit and produce a circuit layout including netlist files (col. 1, lines 24-39),

a synthesis plan library having a set of synthesis plans for at least one circuit, each synthesis plan having a circuit design and a set of parameterized values regarding any of physical characteristics and values of circuit elements (col. 2, lines 42-52, col. 3, lines 2-20, col. 4, lines 49-67, cols. 5-7, Figs. 2-6), being created by

means for determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, col. 10, for example). Such circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 12, Hamid discloses netlists which would include non-sized ones for the design optimization process, design topology for the design and placement, synthesis model, etc. as claimed (Fig. 2-6, for example).

As per claim 13, Hamid discloses synthesis engine including a plurality of synthesis plans (Fig. 1, Summary of the Invention), and tool selecting means for selecting design tools for the synthesis plan for parameterized cells and cell design (Background of the Invention, and col. 3, lines 28-30, for example).

As per claim 14, Hamid discloses a plurality of tools for design optimization, such tools includes simulator, plans for simulation optimizer, etc. (Fig. , col. 5, lines 17-30).

As per claims 15 and 16, Hamid discloses analog components used in the circuit design and optimization.

As per claim 17, Hamid discloses a method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the method of planning a circuit synthesis includes steps and means:

determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

a plurality of synthesis plans for circuit design (Fig. 2, col. 3, lines 27-30),

means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plans (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, for example). Such circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the

design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 18, Hamid discloses tabular forms that correlate each of the set of points to a corresponding result of the simulation.

As per claim 19, Barford teaches polynomial fitted transfer equation over a design parameter values (col. 3, line 46 to col. 4, line 18, col. 10, lines 18-25).

As per claim 20, Hamid discloses analog components in the design.

As per claim 21, Hamid discloses a method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Summary of the Invention). According to Hamid, the method of planning a circuit synthesis includes steps and means:

determining circuit design comprising at least one set of circuit elements (col. 4, lines 49-67, col. 5, lines 1-29, for example), means for identifying a set of parameters for construction of the circuit elements (col. 7, lines 11-27, for example),

means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (cols. 7-16) for circuit elements or cells characterization,

means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (cols. 18-19). Hamid discloses cell characterization by performing simulation over a set of points, but does not explicitly disclose each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches

method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior by polynomial curve fitting function (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, for example). Such circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design and simulation as disclosed in Hamid to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 22, Hamid discloses tabular forms being used to store design and simulation data.

As per claim 23, Barford teaches polynomial fitted function to fit design parameter changes (cols. 3 and 10).

As per claim 24, the art of record, Hamid and Barford, discloses analog components.

Response to Arguments

6. Applicant's arguments with respect to claims 1-10 and 12-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,381,564 B1, issued to Davis et al, on Apr. 2002

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for formal communications intended for entry)

Or:

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

December 1, 2003

Thai Phan
Patent Examiner
Thai Phan
AU: 2123